ABSTRACT

On implementation of the invention provides a stackable chip-scale package for improving memory density that may be mounted within a limited area or module. A novel staggered routing scheme enables the use of the same trace routing at every level of the stacked architecture for efficiently accessing individual memory devices in a chip-scale package stack. The use of a ball grid array chip-scale package architecture in combination with thermally compatible materials decreases the risk of thermal cracking while improving heat dissipation. Moreover, this architecture permits mounting support components, such as capacitors and resistors, on the chip-scale package.